EE/CprE/SE 492 Status Report 3
Feb 12– Feb 26

Group number: **22**

Project title: **ReRAM Compute Asic Fabrication**

Client &/Advisor: **Cheng Wang & Henry Duwe**

Team Members/Role:

Ali Mannan
Tyler Kloser
Austin Miller
Vinicius Malaman Soares

- **Weekly Summary**
  - Working in parallel on four different components. Transimpedance amplifier, flash analog-to=digital converter, 1T1R layout with ReRAM instantiation in layout, and a completed pre-check inverter with the new ChipFoundry CLI tool. Corresponded with other Analog VLSI design team about resistor sizing and the discrepancies between actual behavior and documentation. Scheduled meeting with one of the previous ReRAM senior design members to talk about layout issues.
- **Past week accomplishments**
  - Vinicius Malaman Soares: Worked on trying to get past team's ADC to simulate, did not work. Looked into ADC schematic design we can use. Spent some time using magic, that will be used for the ADC layout in the future.
  - Tyler Kloser: Worked on passing our inverter through precheck and looked at another teams analog mux
  - Ali Mannan: Completed transimpedance amplifier layout with DRC and LVS passing. Ran into issues with LVS, and had to spend significant amount of time redoing the schematic to fix the issues. Extracted parasitic resistances and capacitances, began some work on testing behavior of extracted TIA.
  - Austin Miller: Got module with reram cell finished in layout, LVS ran, but some problems. In communication with others in open-source chip design community for help. Scheduled meeting with previous reram team member for additional questions and help
- **Pending issues**
  - Tyler Kloser: Precheck is freezing when I have the inverter in the wrapper.
  - Ali Mannan: N/A
  - Austin Miller: reram cells do not pass LVS correctly, DRC is all good though
  - Vinicius Malaman Soares:

- **Individual contributions**

NAME	Individual Contributions	Hours this period	HOURS cumulative
Tyler Kloser	Trying to get inverter through precheck	8	19
Ali Mannan	TIA layout completed. TIA parasitics extracted, with post-extraction testing underway	15	33
Austin Miller	Single Reram cell layout, reram LVS troubleshooting. Finding resources from community and past problems found online	13	36
Vinicius Malaman Soares	Tried testing past team's Data Converter, looked at the schematic needed to built said converter and spent time familiarizing myself with magic	10	23

- **Comments and extended discussion**
    - N/A

Plans for the upcoming week

- Ali Mannan: Complete testing of extracted TIA, and integrate TIA into Caravel harness (final step for the TIA component, before pre-check)
- Tyler Kloser: Figure out why precheck is freezing and get the inverter in the wrapper through precheck. Test the analog mux and see if revisions are necessary.
- Austin Miller: Get any module with reram through layout (passing LVS). Discuss previous problems with past team member and community members
- Vinicius Malaman Soares: Create ADC schematic.

- **Summary of weekly advisor meeting**
    - Parallel work is good
    - Try to reuse components where possible (e.g., use the operational amplifier from the TIA as the comparator for flash ADC)
    - Analog design team also has reservations about resistor sizing in the PDK, and has pointed out that the sheet resistance in the documentation does not match the resistance seen on schematic in XSchem.